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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,297	12/31/2003	Jin-Hong Ahn	51876P540	9786

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EXAMINER	
NGUYEN, DANG T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,297	AHN ET AL.	
	Examiner	Art Unit	
	Dang T Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9-11 and 28-33* is/are rejected.

7)☒ Claim(s) *4-8 and 12-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search history*.

DETAILED ACTION

1. This action is responsive to the following communications: the Application filed on December 31, 2003.

2. Claims 1 – 33 are pending in this case. Claims 1, 28, and 31 are independent claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 9-17 recites the limitation wherein "the step (A-2)" in claim 1. There is insufficient antecedent basis for this limitation in the claim.

No antecedent basis for "the step (A-2)" provided by claim 1. It is appear to examiner that claim 2 is providing proper antecedent basis for claims 9-17.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 - 3, 9 - 11, 28, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Takeuchi et al., U.S. Patent No. 5,455,786 – filed Oct. 3, 1995.

Regarding independent claim 1, Fig. 1 of Takeuchi discloses a method for operating a non-volatile (Col. 1 lines 7 – 8) dynamic random access memory (Col. 1 lines 25 – 26)) device including a plurality of memory cells (M1's), each cell having a capacitor (Cs) and a transistor (transistor of M1) having a floating gate (Gate of transistor in M1), comprising the steps of:

(A) preparing a power-on mode for performing a DRAM operation (Col. 4 lines 20-25); and

(B) preparing a power-off mode for holding stored data in the memory cell (Col. 2 lines 5-10).

Regarding dependent claim 2, Takeuchi disclsoes wherein the step (A) includes the steps of:

(A-1) storing data hold in the floating gate into the capacitor (Col. 7 lines 32-39); and

(A-2) adjusting threshold voltage of the transistor all of the memory cell to a first threshold voltage (Col. 4 line 31 – Col. 5 line 29).

Regarding dependent claim 3, Takeuchi discloses wherein the step (B) includes the step of (B-1) moving the data stored in the capacitor to the floating gate (Col. 2 lines 25-40).

Regarding dependent claim 9, Takeuchi discloses the steps of:

a) supplying all gates of the transistors in all of the memory cells (Fig. 1) with a first predetermined voltage in order for fulfilling electrons in the floating gate (Col. 2 lines 20-22); charging all of the capacitors in all of the memory cells (Col. 4 lines 34-35); decreasing the threshold voltage of the transistors to the first threshold voltage (Col. 4 lines 32-40).

Regarding dependent claim 10, Takeuchi discloses the steps of: backing up the captured data in the capacitor (Col. 10 lines 2-7); and restoring the backup data in the capacitor (Col. 10 lines 2-7).

Regarding dependent claim 11, Takeuchi discloses the steps of: supplying one side of the capacitor with about 0V (Col. 4 lines 13-15); and supplying the bit line with the logic HIGH datum (Col. 2 lines 44- 45 discloses data line are set with Vcc/2).

Regarding independent claim 28, Fig. 1 of Takeuchi et al. discloses a non-volatile (Col. 1 lines 7 – 8) dynamic random access memory (Col. 1 lines 25 – 26) device including a plurality of memory cells (M1's) in a matrix (Fig. 1), wherein each memory cell includes: a control gate layer (Horizontal line of Fig. 1 is a control gate layer) coupled to a word line (WLi); a capacitor (Cs) for storing data; a floating transistor (Transistor in M1) for transmitting the stored data in the capacitor to a bit line (DLj); and a first insulating layer (PL1) between the control gate layer and the gate of the floating transistor (transistor in M1), wherein one side of the capacitor is coupled to a drain of the floating transistor and the other side of the capacitor is supplied with a different voltage (Ground) in response to operation mode.

Regarding independent claim 31, Fig. 1 of Takeuchi et al. discloses memory including a plurality of memory cells in a matrix (M1's), wherein each memory cell (M1) includes: a control gate layer (Gate of transistor in M1) coupled to a word line (WLi); a capacitor (Cs) for storing data; and a floating transistor (transistor in M1) for transmitting the stored data in the capacitor to a bit line (DLi), wherein one side of the capacitor is coupled to a drain of the floating transistor (See M1) and the other side is supplied with a different voltage (Ground) in response to the operation mode.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 29 - 30 and 32 - 33 are rejected under 103(a) as being unpatentable over Takeuchi et al., U.S. Patent No. 5,455,786, filed Jun. 9, 1994 in view of Rodgers U.S. Patent No. 4,446,536, filed Jun. 21, 1982.

Regarding dependent claims 29-30 and 32-33, Fig. 1 of Takeuchi et al. as applied to claims 28 and 31 above, fails to disclose device wherein the gate of the floating transistor is made of nitride formed in a single layer serves as a data storage.

Fig. 4 of Rodgers discloses a nonvolatile memory device using single layer floating gate is made of nitrite formed and serves as a data storage (lines 1 – 5 of Abstract; or Col. 1 lines 10 – 12).

Takeuchi and Rodgers et al. are common subject matter for nonvolatile memory using floating gate transistor. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the floating transistor of Takeuchi with the nitrite gate transistor taught by Rodgers et al. for the purpose of accomplishing utilizing Metal Nitride Oxide Semiconductors (MNOS) or "floating gate" transistors for data storage (Rodgers, Col. 1 lines 10 – 13).

Allowable Subject Matter

6. Claims 4 – 8 and 12 - 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With respect to claim 4, in addition to other elements in the respective claim, the prior art does not teach or suggest "wherein storing data hold in the floating gate into the capacitor includes the steps of charging the capacitors of all memory cell with a logic HIGH datum; and discharging the capacitor in the memory cell having the transistor, its floating gate storing a logic high datum"

With respect to claim 12, in addition to other elements in the claim, the prior art does not teach or suggest "removing electrons in the floating gate of the memory cells; discharging the capacitor by supplying gate of the transistor in the memory cells, with the first threshold voltage, and repeat until all of the capacitors is discharged".

With respect to claim 18, in addition to other elements in the claim, the prior art does not teach or suggest "removing electrons in the floating gate of the memory cell storing a logic High datum; discharging the capacitor by supplying gate of the transistor in all of the memory cells with a second threshold voltage, and repeating until all of the capacitors is discharged".

With respect to claim 24, in addition to other elements in the claim, the prior art does not teach or suggest "supplying the word line with a voltage $V_{wl} = V_{blp} + (V_{th+H} + V_{th-L})/2$ Where V_{blp} is a bit line prcharge voltage, V_{th+H} is a first threshold, and V_{th-L} is a second threshold voltage; and writing logic HIGH or LOW data in the capacitor in response to whether the threshold voltage is the V_{th+H} or the V_{th-L}".

Prior art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takata et al.	Patent No. US 5,703,804	Date of Patent: Dec. 30, 1997
Lin et al.	Patent No. US 6,829,166 B2	Date of Patent: Dec. 7, 2004

Contact Information

8. Any inquiry concerning this communication from the examiner should be directed to Dang Nguyen, who can be reached by telephone at (571) 272-1955. Normal contact times are M-F, 8:00 AM - 4:30 PM.

Upon an unsuccessful attempt to contact the examiner, the examiner's supervisor, Richard Elms, may be reached at (571) 272-1869.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is (703) 305-3900. The faxed phone number for organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the Status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC@uspto.gov.

Dang Nguyen 2/2/2005

RICHARD ELMS
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